

U.S. Department of Commerce, Patent and Trademark Office  <b>LIST OF RELEVANT ART CITED BY APPLICANT</b> (Use several sheets if necessary)				Docket No.: 8201/Y01/SYNX/JW		Serial No.: 10/764,620	
<div style="position: relative; height: 100px;"> <div style="position: absolute; top: 0; left: 0; width: 100%; height: 100%; border: 1px solid black; border-radius: 50%; text-align: center; color: black; font-weight: bold; font-size: 1.2em;">             OIPE              NOV 07 2005              U.S. PATENT &amp; TRADEMARK OFFICE           </div> </div>				Applicants: Michael R. Rice, et al			
				Filing Date: January 26, 2004		Group: 2125	

U.S. Patent Documents							
*Examiner Initial	Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate	
CK	US-1	5,544,350	Hung et al.				
CK	US-2	5,612,886	Yi-Cherng Weng				
CK	US-3	5,818,716	Chin et al.				
CK	US-4	5,825,650	Tza-Huei Wang				
CK	US-5	5,971,585	Dangat et al.				
CK	US-6	6,128,588	Guillermo Rudolfo Chacon				
CK	US-7	6,196,001	Tannous et al.				
CK	US-8	6,415,260	Yang et al.				
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CK	F-1	JP 55091839 A	07/11/80	Japan		Abstract		
CK	F-2	JP 58028860 A	02/19/83	Japan		Abstract		
CK	F-3	JP 60049623 A	03/18/85	Japan		Abstract		
CK	F-4	JP 01181156 A	07/19/89	Japan		Abstract		
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CK	OT-1 Przewlocki, H. et al., "DIASTEMOS-computerized system of IC manufacturing control and diagnostics", 1990, Elektronika, Vol. 31 No. 11-12, Pgs. 38-40, Polish Language. (Abstract only)
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CK	OT-3 Prasad, K., "A generic computer simulation model to characterize photolithography manufacturing area in an IC FAB facility", Sept. 1991, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 14 No. 3, Pg. 483-7.

Examiner: <i>Chadi Koyu</i>	Date Considered: <i>12/9/05</i>
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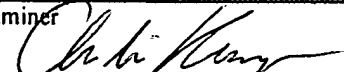
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CK	F-6	JP 02015647 A	01/19/90	Japan			Abstract	
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CK	F-9	JP 06260545 A	09/16/94	Japan			Abstract	
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CK	OT-5	Lou, S. et al., "Using simulation to test the robustness of various existing production control policies", 1991, 1991 Winter Simulation Conference Proceedings, IEEE, Pg. 261-9.
CK	OT-6	Berg, R. et al., "The formula: world class manufacturing for hybrid thin-film component production", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pgs. 53-60.

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## Foreign Patent Documents

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<del>CK</del>	<del>F-14</del>	<del>JP 11296208 A</del>	<del>10/29/99</del>	<del>Japan</del>			<del>Abstract</del>	
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CK	OT-7	Naguib, H., "The implementation of total quality management in a semiconductor manufacturing operation", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 63-7.
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Examiner <i>Chait King</i>	Date Considered 12/9/05
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	Document Number	Date	Country	Class	Subclass	Yes	No	
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CK	OT-11 Leonovich, G., " An approach for optimizing WIP/cycle time/output in a semiconductor fabricator", 1994, Sixteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. 'Low-Cost Manufacturing Technologies for Tomorrow's Global Economy'. Proceedings 1994 IEMT Symposium, Vol. 1, Pg. 108-11.
CK	OT-12 Schomig, A. K. et al., "Performance modelling of pull manufacturing systems with batch servers", 1995, Proceedings 1995 INRIA/IEEE Symposium on Emerging Technologies and Factory Automation. ETFA '95, Vol. 3, Pg. 175-83.

Examiner: <i>Christi Kung</i>	Date Considered: <i>12/9/05</i>
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OK	OT-13	Juba, R. C. et al., "Production improvements using a forward scheduler", 1996, Seventeenth IEEE/CPMT International Electronics Manufacturing Technology Symposium 'Manufacturing Technologies - Present and Future', Pg. 205-9.
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CK	OT-16	Lopez, M. J. et al., "Performance models of systems of multiple cluster tools", 1996, Nineteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1996 IEMT Symposium, Pgs. 57-65.
CK	OT-17	Collins, D. W. et al., "Implementation of Minimum Inventory Variability Scheduling 1-Step Ahead Policy(R) in a large semiconductor manufacturing facility", 1997, 1997 IEEE 6th International Conference on Emerging Technologies and Factory Automation Proceedings, Pgs. 497-504.
CK	OT-18	Labanowski, L., "Improving overall fabricator performance using the continuous improvement methodology", 1997, 1997 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop. Theme - The Quest for Semiconductor Manufacturing Excellence: Leading the Charge into the 21st Century. ASMC Proceedings, Pg. 405-9.

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CR	OT-22	Rose, O., " WIP evolution of a semiconductor factory after a bottleneck workcenter breakdown", 1998, 1998 Winter Simulation Conference. Proceedings, Vol. 2, Pgs. 997-1003.
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CK	OT-24	Weiss, M., "New twists on 300 mm fab design and layout", July 1999, Semiconductor International, Vol. 22 No. 8, Pgs. 103-4, 106, 108.


Examiner <i>Charles H. Wang</i>	Date Considered 12/9/05
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CK	OT-19	Dudde, R. et al., "Flexible data registration and automation in semiconductor production", 1997, Proceedings of the SPIE - The International Society for Optical Engineering, Pg. 171-81.
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ERK	OT-25 Van Antwerp, K. et al., "Improving work-in-progress visibility with active product tags YASIC manufacture", Oct. 1999, Micro, Vol. 17 No. 9, Pgs. 67-9, 72-3.
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CK	OT-27 Martin, D. P., "Capacity and cycle time-throughput understanding system (CAC-TUS) an analysis tool to determine the components of capacity and cycle time in a semiconductor manufacturing line", 1999, 10th Annual IEEE/SEMI. Advanced Semiconductor Manufacturing Conference and Workshop. ASMC 99 Proceedings, Pg. 127-31.

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CK	OT-29	Chen, J. C. et al., "Capacity planning for a twin fab", 1999, 1999 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, Pg. 317-20.
CK	OT-30	Wei Jun-Hu et al., "Optimization methodology in simulation-based scheduling for semiconductor manufacturing", Oct. 2000, Information and Control, Vol. 29 No. 5, Pg. 425-30, Chinese language. (Abstract only)

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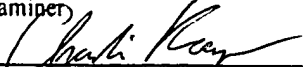
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CK	OT-33	Saito, K. et al., "A simulation study on periodical priority dispatching of WIP for product-mix fabrication", 2002, 13th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference. Advancing the Science and Technology of Semiconductor Manufacturing. ASMC 2002, Pg. 33-7.

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CK	OT-35	Wei Jie Lee, "Optimize WIP scale through simulation approach with WIP, turn-over rate and cycle time regression analysis in semiconductor fabrication", 2002, 2002 Semiconductor Manufacturing Technology Workshop, Pg. 299-301.
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CK	OT-38	Anon, " Wafer level automation", Jan. 1995, European Semiconductor, Vol. 17 No. 1, Pg. 2.
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U.S. Department of Commerce, Patent and Trademark Office  <b>LIST OF RELEVANT ART CITED BY APPLICANT</b> (Use several sheets if necessary)	Docket No.: 8201/Y01/SYNX/JW	Serial No.: 10/764,620
	Applicants: Michael R. Rice, et al	
	Filing Date: January 26, 2004	Group: 2125

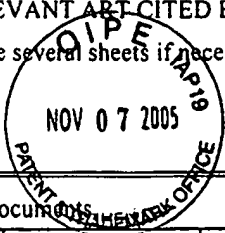
U.S. Patent Documents							
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		US-145					
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		US-151					
		US-152					
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		US-154					

Foreign Patent Documents							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
		F-66						
		F-67						
		F-68						
		F-69						
		F-70						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
CK	OT-40	Pierce, Neal G. et al., " Dynamic dispatch and graphical monitoring system", 1999, IEEE International Symposium on Semiconductor Manufacturing Conference, Proceedings 1999, Pg. 65-68.
CK	OT-41	Nagesh, Sukhi et al., " Intelligent second-generation MES solutions for 300mm fabs", 2000, Solid State Technology, Vol. 43 No. 6, Pgs. 133-134, 136, 138.
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Examiner <i>Charles Kasper</i>	Date Considered 12/9/05
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*Examiner Initial	Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate	
CK	US-1	5,256,204	10/26/93 Hong J. Wu				
CK	US-2	5,668,056	09/16/97 Wu et al.				
CK	US-3	5,976,199	11/02/99 Wu et al.				
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	US-5						
	US-6						
	US-7						
	US-8						
	US-9						
	US-10						
	US-11						


  

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	Document Number	Date	Country	Class	Subclass	Yes	No	
CK	F-1 JP 2000012646 A2	01/14/00	Japan			Abstract Only		
	F-2							
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CK	OT-1	"300mm single-wafer transport", July 1999, Solid State Technology - semiconductor manufacturing and wafer fabrication, Semicon West '99 Product Spotlight, pg. 5.
CK	OT-2	"300mm single-wafer handling", April 2000, Solid State Technology, Product News, <www.solid-state.com>, pg. 99.
CK	OT-3	Griessing, Juergen et al., "Assessing the feasibility of a 300-mm test and monitor wafer handling and logistics system", July 2000, Micro: The 300-mm Imperative, pgs. 1-19.

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	US-13						
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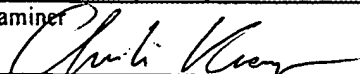
## Foreign Patent Documents

## Translation

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	F-6							
	F-7							
	F-8							
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	F-10							

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CK	OT-4	"The Leading Company in Micro environment", January 3, 2002, Incam Solutions Company, pgs. 1-2.
CK	OT-5	"Improved wafer isolation and additional flexibility", January 3, 2002, Incam Solutions Company SWIF technology, pgs. 1-2.
CK	OT-6	"SEMI standards compliance" and "Related SEMI standards", January 3, 2002, Incam Solutions Related standards, pg. 1.

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	US-32						
	US-33						

Foreign Patent Documents							Translation	
Document Number	Date	Country	Class	Subclass	Yes	No		
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F-12								
F-13								
F-14								
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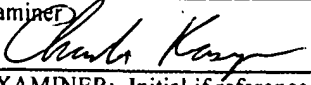
  

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CK	OT-7 "Single Wafer Lots Solution", January 3, 2002, Incam Solutions References, pg. 1.
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OT-9	

Examiner <i>Charles Kerry</i>	Date Considered <i>12/9/05</i>
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U.S. Department of Commerce, Patent and Trademark Office  <div style="display: flex; align-items: center;"> <div style="border: 1px solid black; border-radius: 50%; padding: 10px; text-align: center; margin-right: 10px;">           OIPE AUG 31 2005 PATENT &amp; TRADEMARK OFFICE         </div> <div>           LIST OF RELEVANT ART CITED BY APPLICANT            (Use several sheets if necessary)         </div> </div>				Docket No.: 8201/Y01/SYNX/JW		Serial No.: 10/764,620	
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				Filing Date: January 26, 2004		Group: 2125	
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CK	US-3	6,183,186	02/06/01	Peltola et al.			
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	US-5						
	US-6						
	US-7						
	US-8						
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	US-10						
	US-11						
Foreign Patent Documents							
							Translation
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	F-3						
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	OT-2						
	OT-3						
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				Filing Date: January 26, 2004		Group: 2125	

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CK	US-1	4,401,522	08/30/83	Buschow et al.			
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CK	US-3	4,540,088	09/10/85	Bergh			
CK	US-4	4,650,264	03/17/87	Dahnert			
CK	US-5	4,775,046	10/04/88	Gramarossa et al.			
CK	US-6	6,235,634	05/22/01	Law et al.			
CK	US-7	2002/0090282	07/11/02	Bachrach			
CK	US-8	2003/0010449	01/16/03	Gramarossa et al.			
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	US-10						
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Foreign Patent Documents							Translation	
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	OT-1
	OT-2
	OT-3

Examiner: <i>Charles Key</i>	Date Considered: 12/9/05
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